HELA-10, High IP3, Wide band, Linear Power Amplifier

1.0 Introduction

Communication systems are becoming increasingly complex. Number of carriers used in systems such as CATV is constantly increasing. This complexity increases the inter-modulation products. In order to keep the inter-modulation products under control, the carrier levels need to be lower or the system power output needs to be increased.

Increased output power results in a corresponding increase in DC power consumption and cost. Feed forward amplifiers are used extensively to increase inter-modulation intercept point and thereby decrease the inter-modulation products. Feed forward amplifiers are generally expensive and are not easily available. This product feature presents a new device, HELA-10 which uses a set of balanced amplifiers, which provide high intercept point comparable to feed forward amplifier but at a significantly lower cost.

2.0 HELA-10, A Balanced Power Amplifier

HELA-10 is a balanced, sixteen lead, power amplifier with a nominal gain of 11 dB. Figure 1 shows a photograph of the amplifier. Figure 2 shows the layout of the amplifier with external baluns. It is powered by a single, +12V DC power supply. It operates in Class-A and produces a nominal output power of 1 Watt.

HELA -10 consists of a pair of amplifiers. As they are on the same chip, their gain and phase are very well matched. If a balanced signal is applied to its input, then its output produces a balanced output. By using a set of Baluns at the input and output (Figure 3), a single ended input is first converted into a balanced output in Balun #1, amplified in the amplifiers #1 & #2 and combined in the Balun #2 to produce a single ended output. If the loss of the output balun is zero, the amplifier pair can produce twice the output power of a single amplifier.

Amplifiers are nonlinear. The degree of non-linearity of an amplifier depends on how hard they are driven. Now let us look at the harmonics generated by the amplifier. The phase of the harmonics is related to the phase of the fundamental signal at the input of the amplifier. Let us look at the second harmonic (Figure 4.), the phase at the output is the same. Hence, they get canceled and a second harmonic does not appear at the output of the amplifier. The same is true for all even harmonics. In reality, the amplifiers and baluns are not perfect, hence a small amount of signal is present. HELA-10 has an excellent second order intercept of 88 dBm typical. As the two amplifiers are combined, the power output and odd order intercept point are twice that of the single amplifier.

3.0 Specifications and Performance

Table 1 shows the electrical specifications of the amplifier at room temperature. As can be seen, the power output is typically 30 dBm. A unique feature of this amplifier is its ability to work in both 50 and 75 ohm systems. Mini-Circuits supplies separate sets of Baluns for 75 ohm (MCL part number ADTL1-18-75) and 50 ohm (MCL part number ADTL1-12) systems. Figure 5. Shows the gain and Figure 6 the VSWR of HELA-10 in a 75 ohm system. Gain is extremely flat and it is typically within ±0.4 dB. This is an exellent feature for wideband systems. The VSWR is typically, 1.2:1 showing an excellent match. This meets the stringent matching requirements of a CATV amplifier. Figure 7 shows the output power and Figure 8 the output third order intercept point. Output power is typically 30 dBm (1 watt) over the entire band. IP3 of amplifiers is in general, 10 dB above 1 dB compression. For HELA-10, IP3 is typically 16 dB above 1 dB compression at 150 MHz and 14.7 dB above it at 800 MHz. This is equivalent to using 5 watt amplifier at 150 MHz and 3 Watt at 800 MHz. This high IP3 is of great advantage for use in multi carrier systems.

Figure 9-12 shows the same parameters; Gain, VSWR, Output Power and Output IP3 with 50 S matching circuits. As it can be seen, the gain is very similar to the 75 ohm system and is very flat. Port matching is excellent above 300 MHz and is typically 1.2:1. Below 300 MHz, the VSWR increases to a manageable 2:1. Power output and IP3 are comparable to the 75 ohm version. At cellular frequencies, this amplifier has an excellent IP3 of 45 dBm and delivers 1W of power and excellent port matching. This makes it a superb amplifier for cellular frequencies.

All the referenced graphs and conclusions cover the entire circuit which includes the baluns and the biasing circuits described in 4.0. This amplifier along with the transformers housed in surface mount package makes it an ideal candidate suitable for pick and place and high volume production.

4.0 Performance of HELA-10 as a Cascaded Amplifier

For higher gain applications, a driver amplifier is required. It may not be easy to find a driver having sufficiently high IP3 since the driver contributes to the overall IP3. HELA-10 is a cascadable amplifier. Hence it can also be used as a driver. Figure 13 shows the schematic block diagram of a two stage, cascaded HELA-10 amplifier. A typical gain of 20 dB gain can be achieved using this cascade.

The disadvantage of a direct cascade is the power consumption, which is twice that of a single amplifier. But, HELA-10 has an intelligent biasing scheme to overcome this. By connecting an external shunt resistance from pin #7 to ground the supply current can be controlled. Figure 14 shows the supply current of the amplifier as a function of shunt resistance, which shows the current can be reduced to almost half. Figure 15 shows the 1dB compression versus shunt resistance. Figure 15-1 & 15-2 show Pout at 4 different frequencies vs. shunt resistance and Figure 15-3 & 15-4 show Pout as a function of frequency. A bias resistor value in the range of 10 to 100 ohms reduces the current consumption by 150 to 200 mA and still produces a power output of 27 dBm typically. This is more than adequate as a driver. This feature can also be used to reduce the current consumption when HELA-10 is used for lower power applications. Figure 16-1 and 16-2 show the performance (Gain) over 50 to 1000 MHz using various shunt resistances in 75 ohm and 50 ohm systems. Figure 17-1 and 17-2 show IP3 at various values

of shunt resistance in 75 & 50 ohms respectively. As seen in Figure 16-2, the gain variation is very small, about 0.3 dB. But the output power can be reduced and also the supply current using a standard 1/8 watt resistor.

HELA-10 can also be used at different supply voltages, at customer's discretion. Figure 18 shows the DC current at various supply voltages. Figure 19-1 and 19-2 show the output power in 75 and 50 ohm systems at various supply voltages. Figure 20-1 and 20-2 show the Gain at various supply voltages. Figures 21-1 and 21-2 show the IP3 at 800 MHz at various supply voltages. Table 2 shows a summary of the findings in electrical specifications both in 50 ohm and 75 ohm systems.

5.0 Layout and Thermal Aspects:

The PCB layout for the HELA-10 amplifier must consider both the electrical requirements of the parts (proper line impedance, bypassing, etc.) and the thermal requirements. The thermal requirement, to meet the stated MTTF of better than 800 years, states that the maximum temperature of the heat slug on the bottom of the HELA-10 package is 110°C. There are three different thermal interfaces between the bottom of the HELA-10 and the chassis. The first is the solder connection of the HELA-10 heat slug to the PCB. The second interface is the heat transfer through the PCB, and the third is the PCB to chassis interface.

The first interface, the solder connection of the HELA-10 heat slug to the PCB, should cover the full area of the HELA-10 heat slug for maximum effectiveness.

The PCB must be designed for the maximum expected system ambient temperature. To do this, the following two parameters need to be known: the maximum external ambient temperature and the temperature rise of the chassis above the external ambient temperature.

Once these two parameters are known the maximum temperature rise between the chassis and the HELA-10 can easily be calculated.

Maximum Temperature Rise (°C):	Chassis to HELA-10 slug = 110 - maximum external temperature - chassis rise
For example if:	Maximum external temperature = 60°C Chassis rise due to internal heating = 20°C
Then:	Maximum Temperature Rise (°C): Chassis to HELA-10 slug = 110 - 60 - 20= 30°C

In the above example a 30°C rise is allowed in the PCB mount between the bottom of the HELA-10 slug and the chassis. Knowing this a PCB can be designed that provides a thermal resistance which will maintain a 30°C or less temperature rise.

The second interface is the heat transfer through the PCB. FR4, the typical PCB material used in most applications, has very poor thermal conduction properties and cannot be used without the addition of through via holes under the HELA-10. The via holes should be copper plated and then solder filled for the lowest thermal resistance. The via holes then conduct the heat through the FR4 to the bottom of the PCB, while the FR4 material provides the mechanical support. The thermal resistance of the via holes, given in degree C rise per watt of power dissipation, is a function of via diameter and the thickness of the copper plating on the walls of

the via holes. Tables 3, 4, 5 show the calculated thermal resistance of solder filled, plated though via hole with different via diameter and copper plating thickness. Table 3 shows the thermal resistance with 0.8 mil copper plating, Table 4 with 1 mil, and Table 5 with 2 mil copper plating. The thermal resistance of the copper plating alone is shown in the column Plating, the thermal resistance of the solder fill is shown in the next column and the column labeled combined shows the calculated thermal resistance of both the copper plating and the solder fill for a single via. The next columns show the thermal resistance achieved by using multiple via holes.

As an example, a 32 mil diameter via with 2 mil thick copper plating has the following properties:

> Thermal resistance of the copper plating = 32.5°C / watt
> Thermal resistance of the solder fill = 77.7°C / watt
> Combined thermal resistance of Single Via, a parallel combination of the above = 22.94°C / watt

A thermal resistance of 22.94°C / Watt would produce a 145°C rise with 6.3 Watts of power dissipation (HELA-10) and therefore a single via cannot be used. As more via holes are added, the combined thermal resistance decreases quickly and is determined the same way as for parallel resistors. If we use 36 such via holes the total thermal resistance will be only 0.64°C per Watt and the temperature rise though the PCB will be only 4°C. The actual via diameter, thickness of the copper plating, and number of via holes used will be determined by the limits of the PCB manufacturing process used.

The third interface is between the PCB and the chassis. Note the chassis is considered to be an infinite heat sink in this application note. Unlike the HELA-10 to PCB interface, this cannot be a solder connection due to the mismatch in thermal expansion of the PCB and chassis material and other production problems. A thermally conductive elastomer or gasket material is recommended. One such material that maybe applicable for this application is Thermagon, Inc.'s T-PLI 200 material. This material is a thermally conductive, conformable elastomer that is available in either sheet form or cut to size.

This material should conform to any irregularities on the PCB and chassis surfaces cause by the manufacturing process while providing a low thermal resistance. A sheet thickness of 20 mils appears to be the best compromise between thermal resistance, tolerance build-up, and handling. The 20 mil thick material has a stated thermal resistance of 0.14°C - in2 per Watt. Using a square area of 0.1 square inches at this interface and a power dissipation of 6.3 Watts a temperature rise of 8.8°C is expected. The PCB should be attached to the chassis with screws, providing a slight compression of the elastomer material. The user must determine if this material is acceptable for their application.

By excellent thermal management technique, HELA-10 is kept at less then 110°C. Hence it can be soldered to the PCB with normal solder such as SN60 or SN63 and also can be used at max. ambient temperature of 80°C.

6.0 Environmental Capabilities

As part of qualification, testing HELA-10 amplifier in its 16-lead SOIC package has passed the following environmental tests under the conditions listed below:

Test	Specification	Conditions	Units Passed/failed
Temperature Cycling with Pre-stress	Jedec-Jes22 Method A112 (Pre-stress)	85°C/85°C, 72 hours 230°C peak reflow	90 / 0 (2 lots)
	MIL-STD-883 Method 1010 (Temp Cycle)	-65°C to 165°C 100 cycles Air to Air	
Accelerated Humidity HAST	Jedec-22-A110 without bias	125°C/85%RH 72 hours	90 / 0 (2 lots)
Thermal Shock	MIL-STD-883 Method 1011	-55°C to 125°C 15 cycles Liquid	78 / 0 (2 lots)
Autoclave	Jedec-Jesd22 Test Meth. A102B	121°C/100%RH 72 hrs.	90 / 0 (2 lots)
Solder Reflow Heat	----	One pass belt furnace 220°C peak	90 / 0 (2 lots)

7.0 Conclusion

HELA-10 is a versatile one watt high IP3 (45 dBm) and IP2 (88 dBm) low cost monolithic amplifier. External baluns are required. Balun sets as well as amplifier test boards are offered by Mini-Circuits. The amplifiers are cascadable and perform equally well in both 75 ohms and 50 ohms system. HELA-10 can also be used as a high IP3 low power driver amplifier with reduced maximum power out capability. As a driver, it has a low current mode built into its biasing circuit in order to reduce DC power consumption.

Figure 1 - HELA 10 Photograph

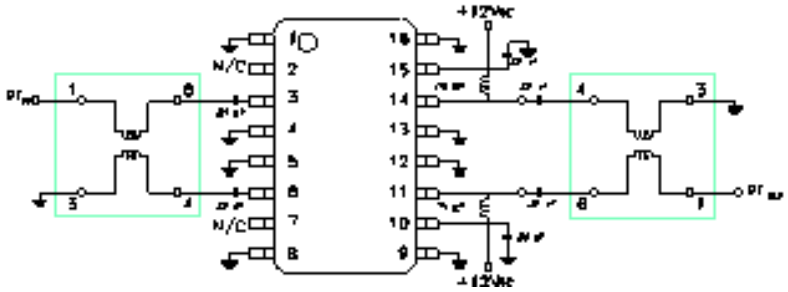

Figure 2 - HELA 10 Layout with External Baluns

.01 µ F Cap is Mini-Circuits Part Number B55-11-103
.75 µ H Choke is Mini-Circuits Part Number B65-C5-751JC

Table 1 - Electrical Specifications at 25°C

FREQ (MHz)	GAIN* (dB)				MAXIMUM POWER (dBm) Output Input (1dB Comp.) (no			DYNAMIC RANGE NF IP3 dB dBm		VSWR*** Typ (:1)		DC POWER		THERMAL RESISTANCE**
	Min.	Typ	Max	Typ Flatness	Typ	Min	damage)	Typ	Typ	In	Out	Volt (V)	Current (mA)	0jc °C/W
50-1000	10	11	13	±0.4	30	26	20	3.5	47	1.22	1.22	12	525	6

* Includes transformer losses at input and output.
** Thermal resistance form junction to heat slug.
*** For 75 ohm. For 50 ohm. VSWR increases from 1.2:1 at 1 GHz to 2.0:1 at 50 MHz.

Table 2

HELA-10	**50 Ohm System**	**75 Ohm System**
Gain vs. **Shunt Resistance**	Gain variation with shunt resistance is minimal and is 0.3 dB typical.	Gain variation with shunt resistance is minimal and is 0.3 dB typical.
P_{out} vs. **Shunt Resistance**	There are 1.5 dB and 2.4 dB improvement on Pout for both low and high frequency range from 10 to 100 ohm and 100 to 1000 ohm Shunt Resistance. Above 1000 ohm Shunt resistance, Pout is almost the same.	There are 1.3 dB and 2.1 dB improvement on Pout for both low and high frequency range from 10 to 100 ohm and 100 to 1000 ohm Shunt Resistance. Above 1000 ohm Shunt resistance, P_{out} is almost the same.
OIP3 vs. **Shunt Resistance**	IP3 increases with increasing shunt resistance (Figure 11).	IP3 increases with increasing shunt resistance (Figure 11).
DC Supply Current vs. **Shunt Resistance**	Current increases with increasing shunt resistance and varies from 250 to 450 mA (Figure 14).	Current increases with decreasing shunt resistance and varies from 250 to 450 mA (Figure 14).
Gain vs. **Supply Voltage**	Gain variation is 0.5 to 1.0 dB from 5 volts to 13 volts.	Gain variation is 0.5 to 1.0 dB from 5 volts to 13 volts.
Max. P_{out} vs. **Supply Voltage**	Max. P_{out} increases from +22 dBm to +32 dBm for device voltages from 4 volts to 13 volts DC.	Similar to 50 ohm system.

DC Current vs. **Supply Voltage**	DC current is proportional to supply voltage.	Similar to 50 ohm system.
OIP3 vs. **Supply Voltage**	OIP3 increases with supply voltage.	Similar to 50 ohm system.
VSWR (Input)	Decreases from 2.6:1 at 50 MHz to 1.2:1 at 300 MHz and beyond.	Very low, 1.2:1 over the entire range
VSWR (Output)	Decreases from 2.6:1 at 50 MHz to 1.2:1 at 300 MHz and beyond.	Very low 1.15:1 over the entire range.

Table 3 - Thermal Resistance of Solder Filled, Plated Thru Via Hole

PCB Thickness	62 mils
Plating Thickness	0.8 mils
Plating Thermal Conductivity	3.98 Watts/cm°C
Fill Conductivity	0.51 Watts/cm°C

Via	Thermal Resistance (°C/Watt)			Multiple Vias					
Dia (Mils)	Plating	Fill	Combined	10	20	30	40	50	60
10	265.2	863.7	202.92	20.29	10.15	6.76	5.07	4.06	3.38
11	239.2	689.7	177.62	17.76	8.88	5.92	4.44	3.55	2.96
12	217.9	563.4	157.12	15.71	7.86	5.24	3.93	3.14	2.62
13	200.0	468.9	140.21	14.02	7.01	4.67	3.51	2.80	2.34
14	184.9	396.3	126.06	12.61	6.30	4.20	3.15	2.52	2.10
15	171.8	339.4	114.08	11.41	5.70	3.80	2.85	2.28	1.90
16	160.5	293.9	103.83	10.38	5.19	3.46	2.60	2.08	1.73
17	150.6	257.0	94.96	9.50	4.75	3.17	2.37	1.90	1.58
18	141.9	226.6	87.24	8.72	4.36	2.91	2.18	1.74	1.45
19	134.1	201.3	80.47	8.05	4.02	2.68	2.01	1.61	1.34
20	127.1	180.0	74.49	7.45	3.72	2.48	1.86	1.49	1.24
21	120.8	161.9	69.19	6.92	3.46	2.31	1.73	1.38	1.15
22	115.1	146.4	64.45	6.44	3.22	2.15	1.61	1.29	1.07
23	109.9	133.1	60.20	6.02	3.01	2.01	1.50	1.20	1.00
24	105.2	121.5	56.37	5.64	2.82	1.88	1.41	1.13	0.94
25	100.8	111.3	52.90	5.29	2.65	1.76	1.32	1.06	0.88
26	96.8	102.4	49.76	4.98	2.49	1.66	1.24	1.00	0.83
27	93.1	94.5	46.90	4.69	2.34	1.56	1.17	0.94	0.78
28	89.7	87.4	44.28	4.43	2.21	1.48	1.11	0.89	0.74
29	86.5	81.2	41.88	4.19	2.09	1.40	1.05	0.84	0.70
30	83.6	75.6	39.68	3.97	1.98	1.32	0.99	0.79	0.66
31	80.8	70.5	37.65	3.77	1.88	1.26	0.94	0.75	0.63
32	78.2	65.9	35.78	3.58	1.79	1.19	0.89	0.72	0.60
33	75.8	61.8	34.04	3.40	1.70	1.13	0.85	0.68	0.57
34	73.5	58.1	32.43	3.24	1.62	1.08	0.81	0.65	0.54
35	71.4	54.6	30.94	3.09	1.55	1.03	0.77	0.62	0.52
36	69.3	51.5	29.55	2.95	1.48	0.98	0.74	0.59	0.49
37	67.4	48.6	28.25	2.82	1.41	0.94	0.71	0.56	0.47
38	65.6	46.0	27.04	2.70	1.35	0.90	0.68	0.54	0.45
39	63.9	43.6	25.90	2.59	1.30	0.86	0.65	0.52	0.43
40	62.3	41.3	24.84	2.48	1.24	0.83	0.62	0.50	0.41
41	60.7	39.3	23.84	2.38	1.19	0.79	0.60	0.48	0.40
42	59.2	37.3	22.90	2.29	1.15	0.76	0.57	0.46	0.38
43	57.8	35.6	22.02	2.20	1.10	0.73	0.55	0.44	0.37
44	56.5	33.9	21.18	2.12	1.06	0.71	0.53	0.42	0.35
45	55.2	32.4	20.40	2.04	1.02	0.68	0.51	0.41	0.34
46	54.0	30.9	19.66	1.97	0.98	0.66	0.49	0.39	0.33
47	52.8	29.6	18.96	1.90	0.95	0.63	0.47	0.38	0.32
48	51.7	28.3	18.29	1.83	0.91	0.61	0.46	0.37	0.30
49	50.6	27.1	17.66	1.77	0.88	0.59	0.44	0.35	0.29
50	49.6	26.0	17.06	1.71	0.85	0.57	0.43	0.34	0.28

Table 4 - Thermal Resistance of Solder Filled, Plated Thru Via Hole

PCB Thickness	62 mils
Plating Thickness	1 mils
Plating Thermal Conductivity	3.98 Watts/cm°C
Fill Conductivity	0.51 Watts/cm°C

Via	Thermal Resistance (°C/Watt)			Multiple Vias					
Dia (Mils)	Plating	Fill	Combined	10	20	30	40	50	60
10	216.9	952.2	176.67	17.67	8.83	5.89	4.42	3.53	2.94
11	195.2	752.3	155.00	15.50	7.75	5.17	3.88	.10	2.58
12	177.5	609.4	137.45	13.74	6.87	4.58	3.44	2.75	2.29
13	162.7	503.6	122.96	12.30	6.15	4.10	3.07	2.46	2.05
14	150.2	423.2	110.84	11.08	5.54	3.69	2.77	2.22	1.85
15	139.4	360.6	100.56	10.06	5.03	3.35	2.51	2.01	1.68
16	130.1	310.9	91.74	9.17	4.59	3.06	2.29	1.83	1.53
17	122.0	270.8	84.12	8.41	4.21	2.80	2.10	1.68	1.40
18	114.8	238.0	77.47	7.75	3.87	2.58	1.94	1.55	1.29
19	108.5	210.9	71.62	7.16	3.58	2.39	1.79	1.43	1.19
20	102.7	188.1	66.45	6.64	3.32	2.21	1.66	1.33	1.11
21	97.6	168.8	61.85	6.18	3.09	2.06	1.55	1.24	1.03
22	93.0	152.3	57.73	5.77	2.89	1.92	1.44	1.15	0.96
23	88.7	138.2	54.04	5.40	2.70	1.80	1.35	1.08	0.90
24	84.9	125.9	50.70	5.07	2.53	1.69	1.27	1.01	0.84
25	81.3	115.2	47.68	4.77	2.38	1.59	1.19	0.95	0.79
26	78.1	105.8	44.93	4.49	2.25	1.50	1.12	0.90	0.75
27	75.1	97.5	42.42	4.24	2.12	1.41	1.06	0.85	0.71
28	72.3	90.1	40.12	4.01	2.01	1.34	1.00	0.80	0.67
29	69.7	83.6	38.01	3.80	1.90	1.27	0.95	0.76	0.63
30	67.3	77.7	36.07	3.61	1.80	1.20	0.90	0.72	0.60
31	65.1	72.5	34.28	3.43	1.71	1.14	0.86	0.69	0.57
32	63.0	67.7	32.63	3.26	1.63	1.09	0.82	0.65	0.54
33	61.0	63.4	31.09	3.11	1.55	1.04	0.78	0.62	0.52
34	59.2	59.5	29.67	2.97	1.48	0.99	0.74	0.59	0.49
35	57.4	56.0	28.34	2.83	1.42	0.94	0.71	0.57	0.47
36	55.8	52.7	27.10	2.71	1.36	0.90	0.68	0.54	0.45
37	54.2	49.7	25.95	2.59	1.30	0.86	0.65	0.52	0.43
38	52.8	47.0	24.86	2.49	1.24	0.83	0.62	0.50	0.41
39	51.4	44.5	23.85	2.38	1.19	0.79	0.60	0.48	0.40
40	50.1	42.2	22.90	2.29	1.14	0.76	0.57	0.46	0.38
41	48.8	40.1	22.00	2.20	1.10	0.73	0.55	0.44	0.37
42	47.6	38.1	21.16	2.12	1.06	0.71	0.53	0.42	0.35
43	46.5	36.3	20.37	2.04	1.02	0.68	0.51	0.41	0.34
44	45.4	34.5	19.62	1.96	.098	0.65	0.49	0.39	0.33
45	44.4	33.0	18.91	1.89	0.95	0.63	0.47	0.38	0.32
46	43.4	31.5	18.24	1.82	0.91	0.61	0.46	0.36	0.30
47	42.4	30.1	17.61	1.76	0.88	0.59	0.44	0.35	0.29
48	41.5	28.8	17.01	1.70	0.85	0.57	0.43	0.34	0.28
49	40.7	27.6	16.44	1.64	0.82	0.55	0.41	0.33	0.27
50	39.8	26.4	15.90	1.59	0.79	0.53	0.40	0.32	0.26

Table 5 Thermal Resistance of Solder Filled, Plated Thru Via Hole

PCB Thickness	62 mils
Plating Thickness	2 mils
Plating Thermal Conductivity	3.98 Watts/cm°C
Fill Conductivity	0.51 Watts/cm°C

Via	Thermal Resistance (°C/Watt)			Multiple Vias					
Dia (Mils)	Plating	Fill	Combined	10	20	30	40	50	60
11	122.0	1692.8	113.81	11.38	5.69	3.79	2.85	2.28	1.90
10	108.5	1243.7	99.76	9.98	4.99	3.33	2.49	2.00	1.66
12	97.6	952.2	88.53	8.85	4.43	2.95	2.21	1.77	1.48
13	88.7	752.3	79.37	7.94	3.97	2.65	1.98	1.59	1.32
14	81.3	609.4	71.76	7.18	3.59	2.39	1.79	1.44	1.20
15	75.1	503.6	65.34	6.53	3.27	2.18	1.63	1.31	1.09
16	69.7	423.2	59.86	9.00	2.99	2.00	1.50	1.20	1.00
17	65.1	360.6	55.13	5.51	2.76	1.84	1.38	1.10	0.92
18	61.0	310.9	51.00	5.10	2.55	1.70	1.27	1.02	0.85
19	57.4	270.8	47.37	4.74	2.37	1.58	1.18	0.95	0.79
20	54.2	238.0	44.17	4.42	2.21	1.47	1.10	0.88	0.74
21	51.4	210.9	41.31	4.13	2.07	1.38	1.03	0.83	0.69
22	48.8	188.1	38.75	3.88	1.94	1.29	0.97	0.78	0.65
23	46.5	168.8	36.45	3.64	1.82	1.21	0.91	0.73	0.61
24	44.4	152.3	34.36	3.44	1.72	1.15	0.86	0.69	0.57
25	42.4	138.2	32.47	3.25	1.62	1.08	0.81	0.65	0.54
26	40.7	125.9	30.74	3.07	1.54	1.02	0.77	0.61	0.51
27	39.0	115.2	29.16	2.92	1.46	0.97	0.73	0.58	0.49
28	37.5	105.8	27.71	2.77	1.39	0.92	0.69	0.55	0.46
29	36.2	97.5	26.37	2.64	1.32	0.88	0.66	0.53	0.44
30	34.9	90.1	25.14	2.51	1.26	0.84	0.63	0.50	0.42
31	33.7	83.6	24.00	2.40	1.20	0.80	0.60	0.48	0.40
32	32.5	77.7	22.94	2.29	1.15	0.76	0.57	0.46	0.38
33	31.5	72.5	21.95	2.19	1.10	0.73	0.55	0.44	0.37
34	30.5	67.7	21.03	2.10	1.05	0.70	0.53	0.42	0.35
35	29.6	63.4	20.17	2.02	1.01	0.67	0.50	0.40	0.34
36	28.7	59.5	19.37	1.94	0.97	0.65	0.48	0.39	0.32
37	27.9	56.0	18.61	1.86	0.93	0.62	0.47	0.37	0.31
38	27.1	52.7	17.90	1.79	0.90	0.60	0.45	0.36	0.30
39	26.4	49.7	17.24	1.72	0.86	0.57	0.43	0.34	0.29
40	25.7	47.0	16.61	1.66	0.83	0.55	0.42	0.33	.028
41	25.0	44.5	16.02	1.60	0.80	0.53	0.40	0.32	0.27
42	24.4	42.2	15.46	1.55	0.77	0.52	0.39	0.31	0.26
43	23.8	40.1	14.93	1.49	0.75	0.50	0.37	0.30	0.25
44	23.2	38.1	14.43	1.44	0.72	0.48	0.36	0.29	0.24
45	22.7	36.3	13.96	1.40	0.70	0.47	0.35	0.28	0.23
46	22.2	34.5	13.51	1.35	0.68	0.45	0.34	0.27	0.23
47	21.7	33.0	13.08	1.31	0.65	0.44	0.33	0.26	0.22
48	21.2	31.5	12.67	1.27	0.63	0.42	0.32	0.25	0.21
49	20.8	30.1	12.29	1.23	0.61	0.41	0.31	0.25	0.20
50	20.3	28.8	11.92	1.19	0.60	0.40	0.30	0.24	0.20

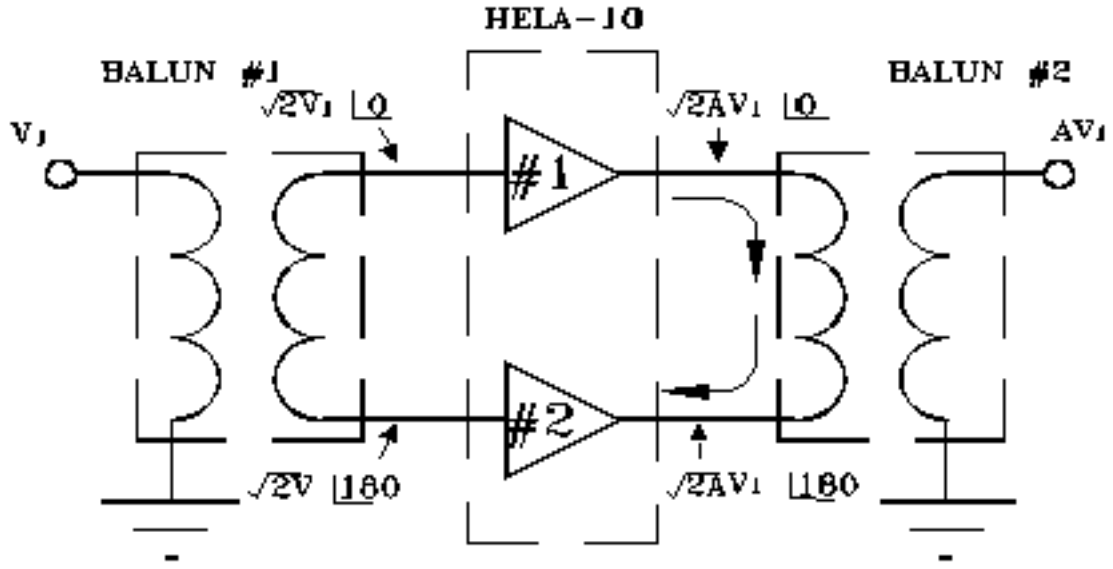

Figure 3

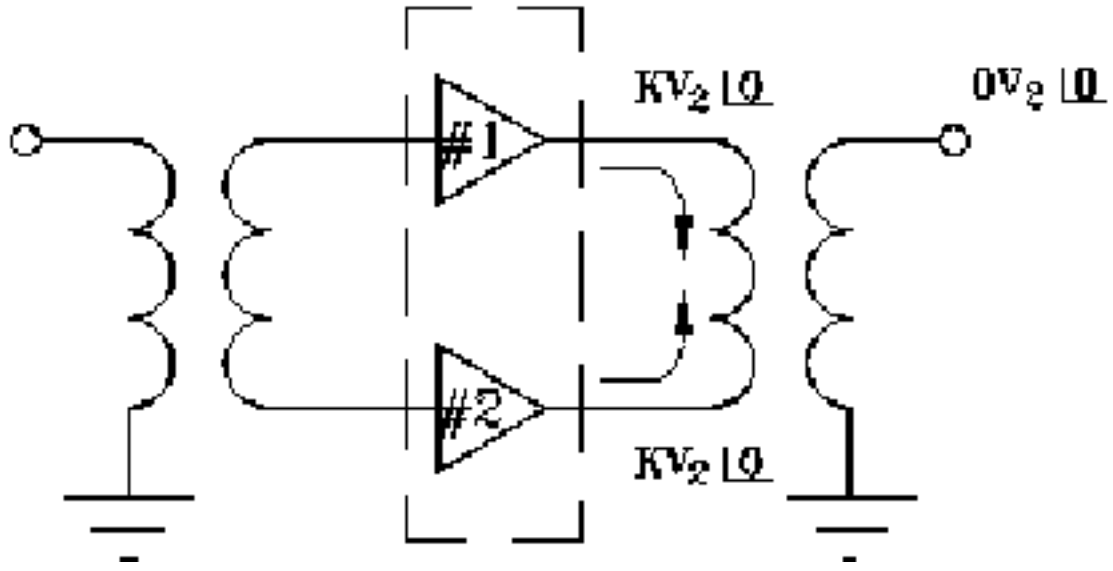

Figure 4-Second Harmonic Cancel

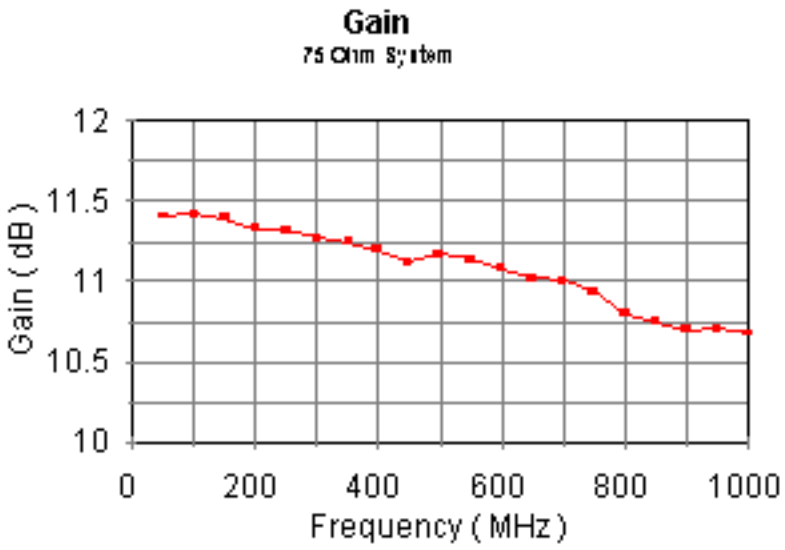

Figure 5

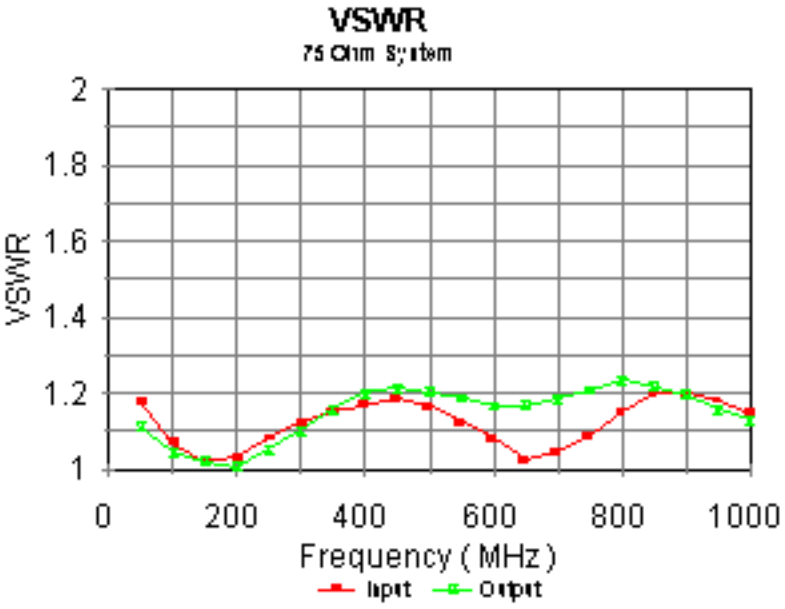

Figure 6

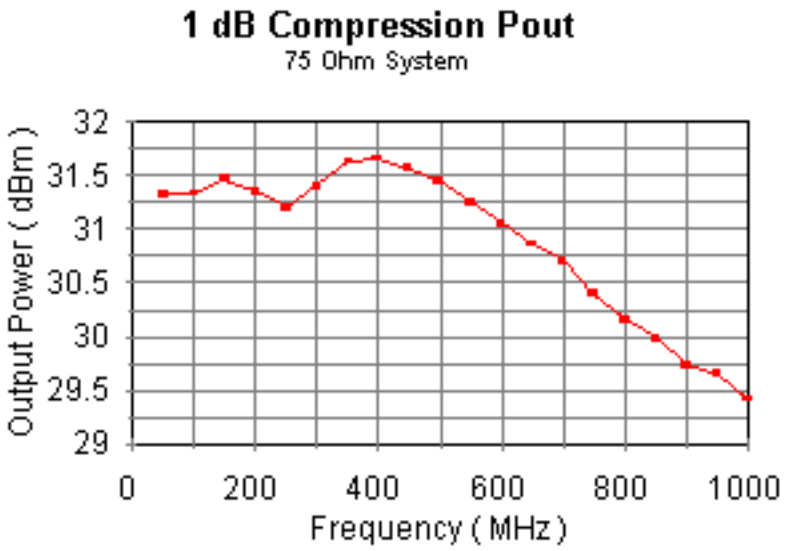

Figure 7

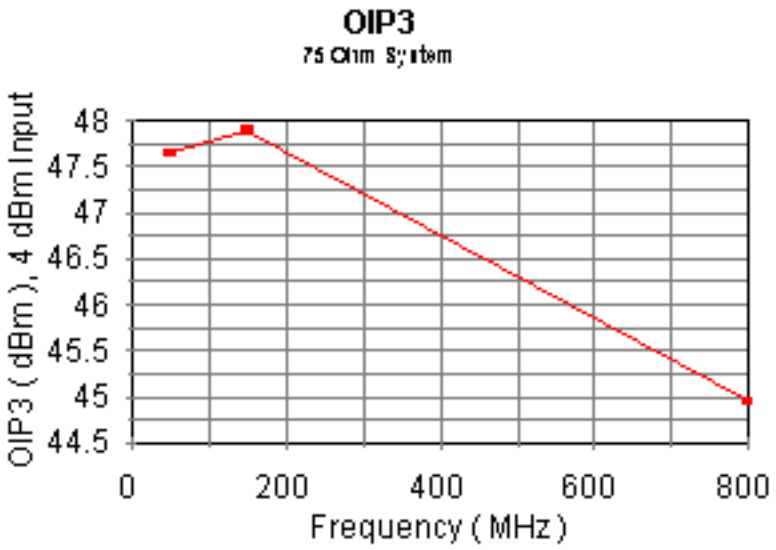

Figure 8

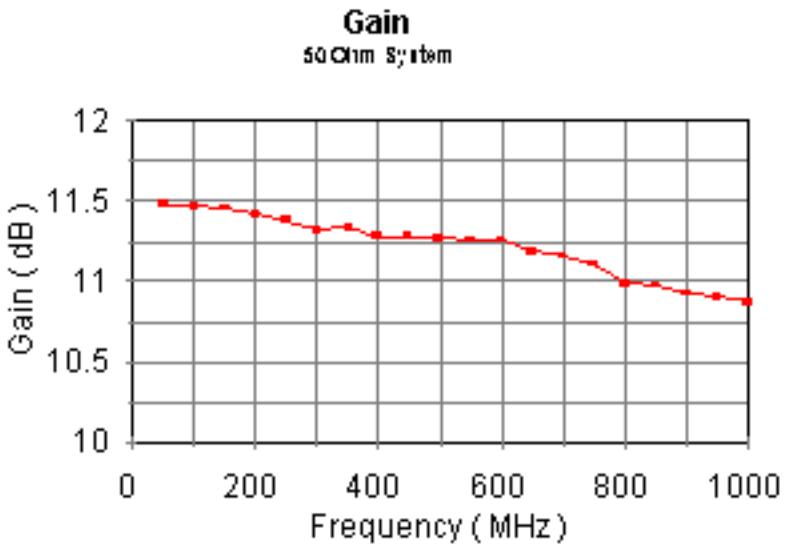

Figure 9

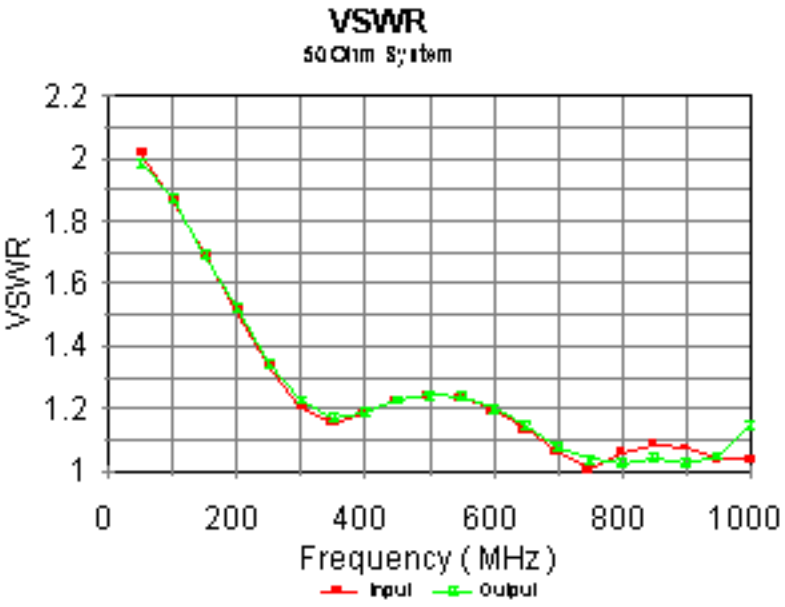

Figure 10

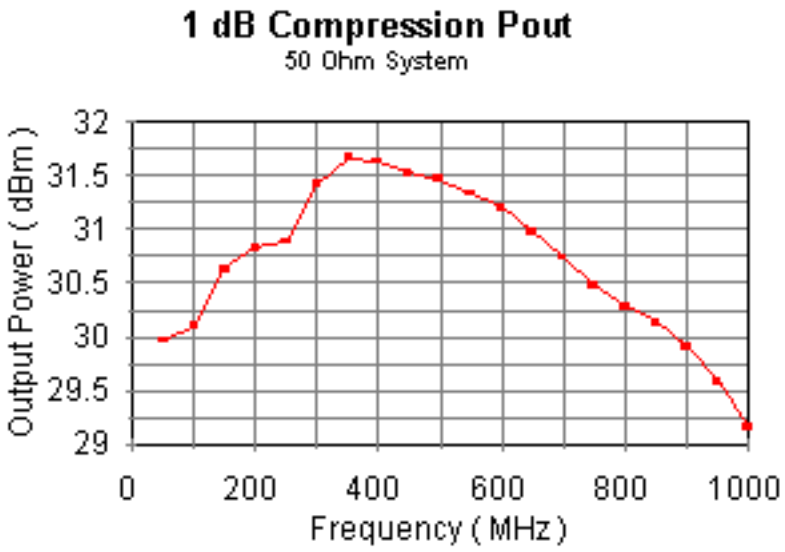

Figure 11

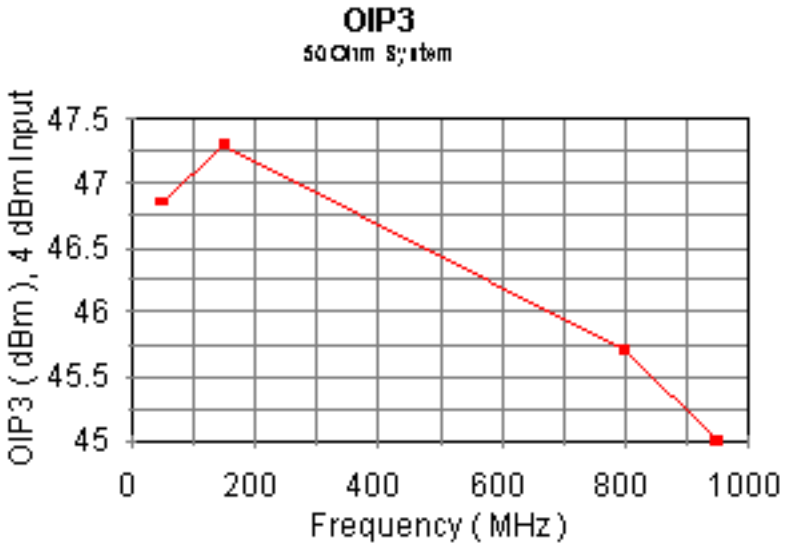

Figure 12

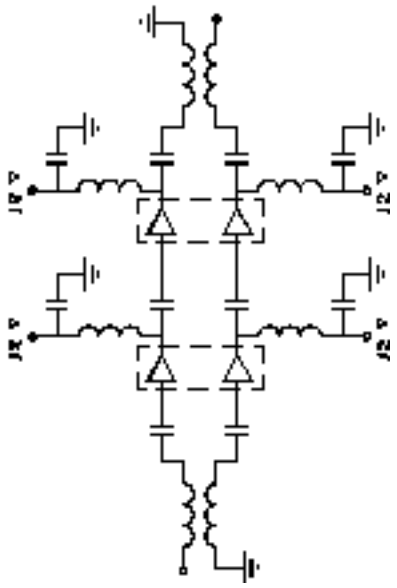

Figure 13

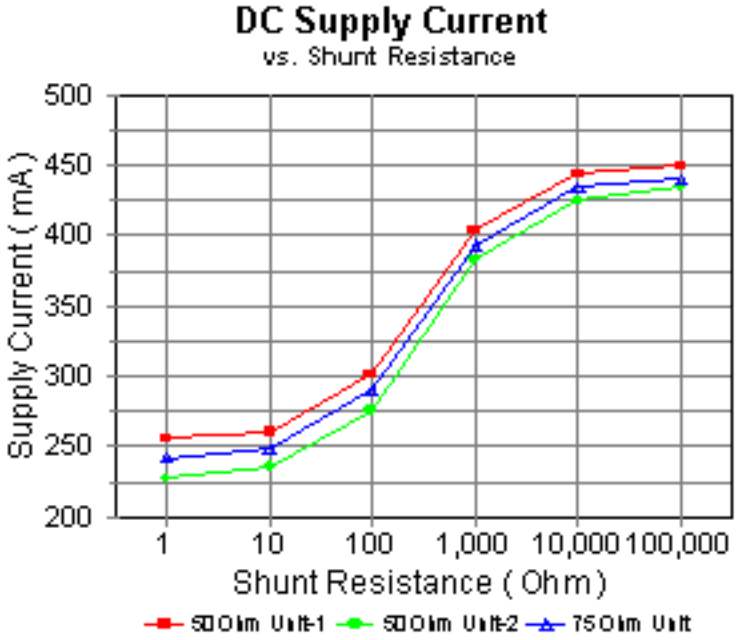

Figure 14

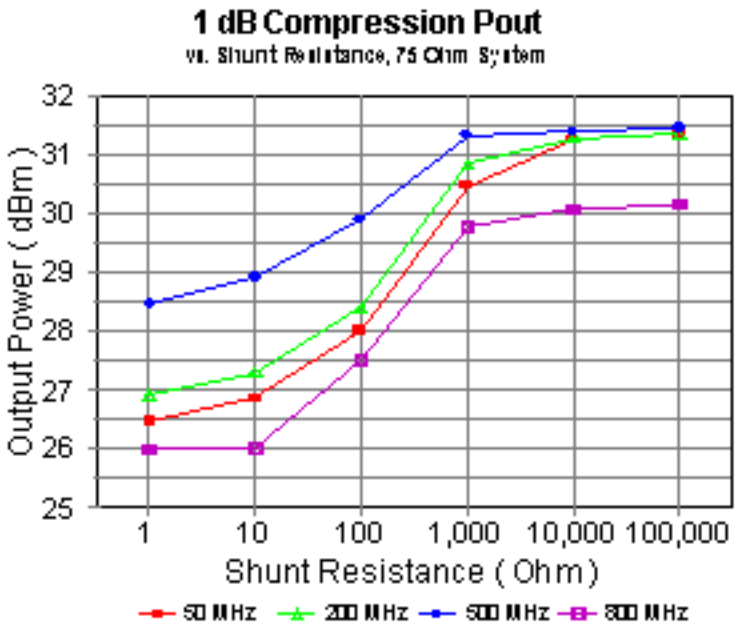

Figure 15-1

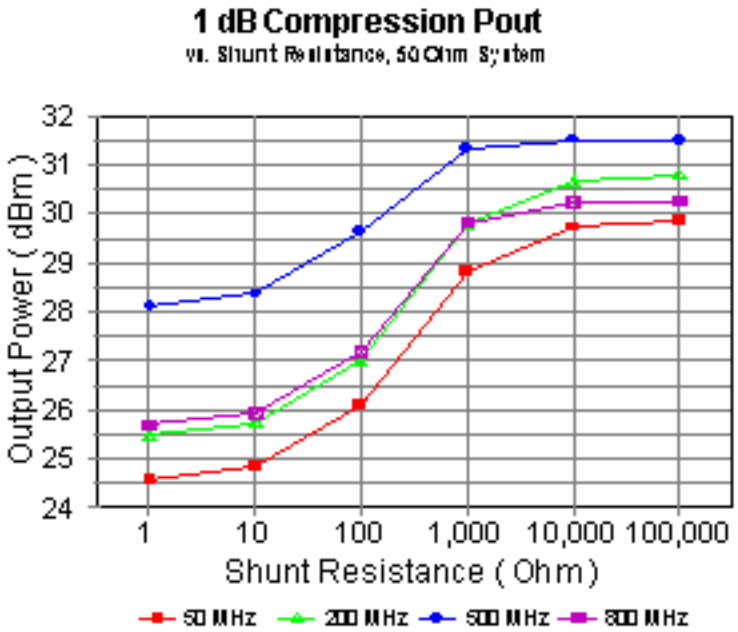

Figure 15-2

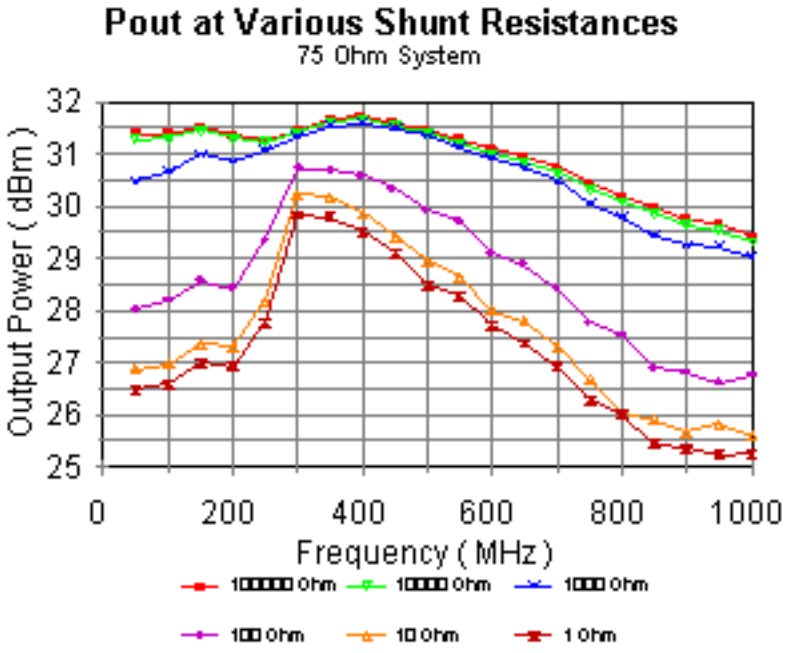

Figure 15-3

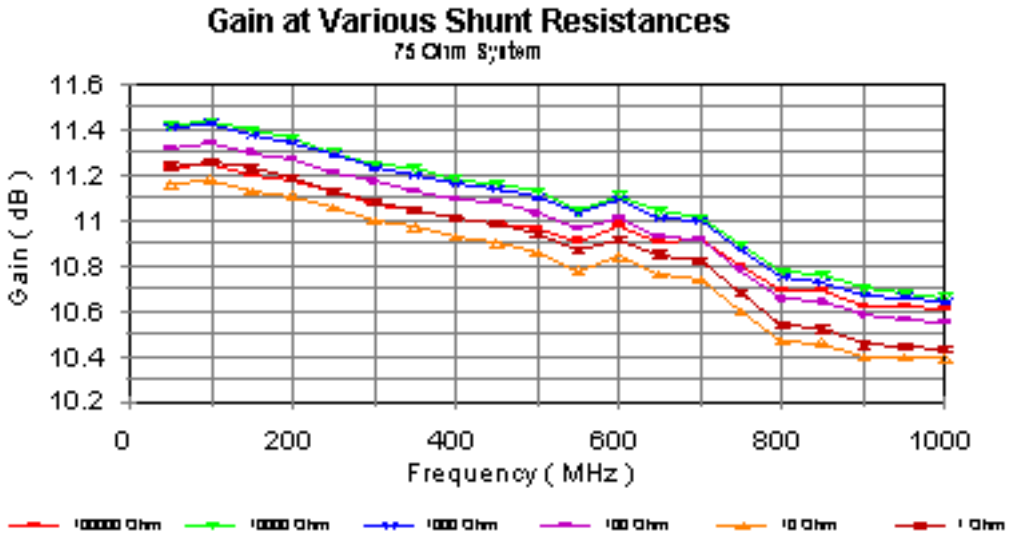

Figure 15-4

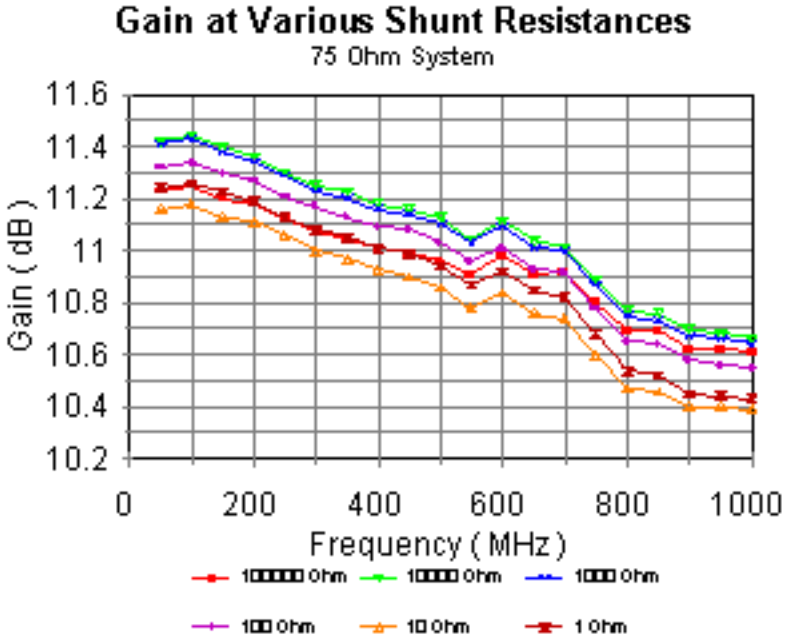

Figure 16-1

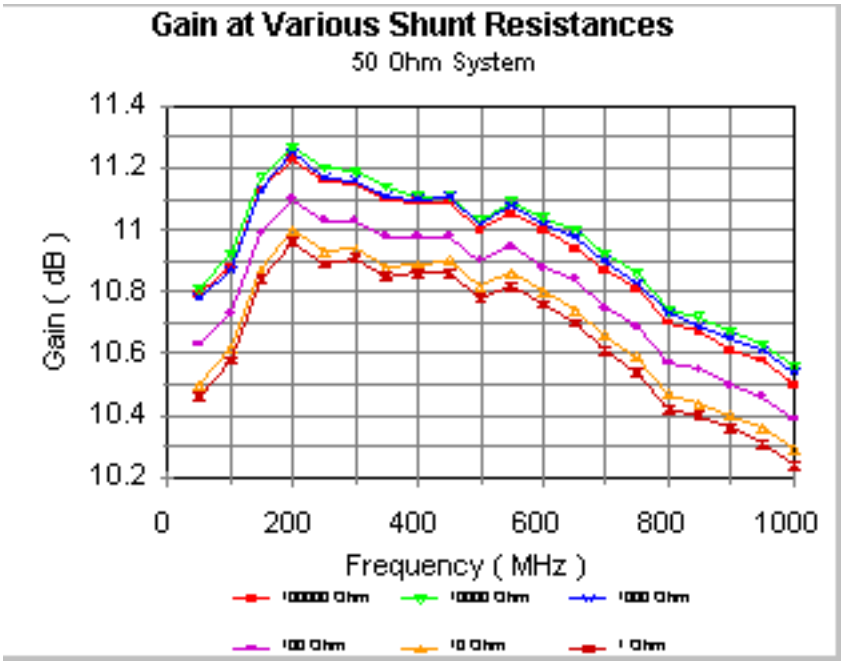

Figure 16-2

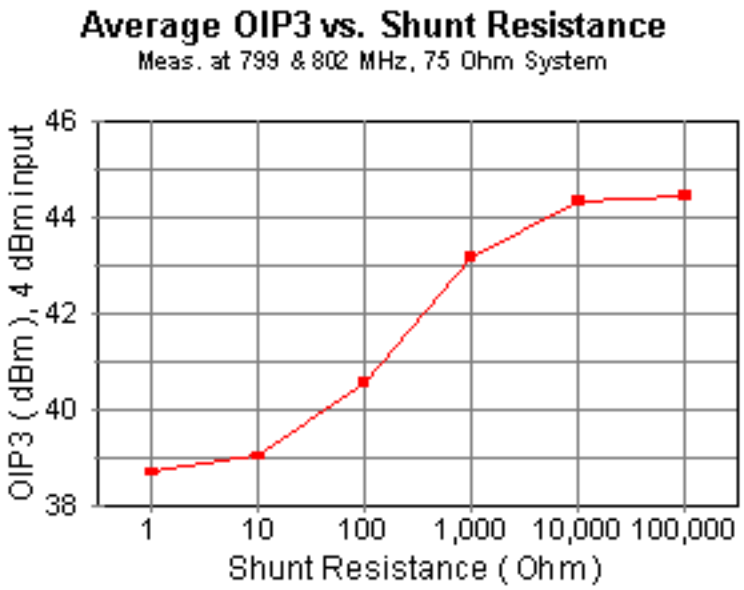

Figure 17-1

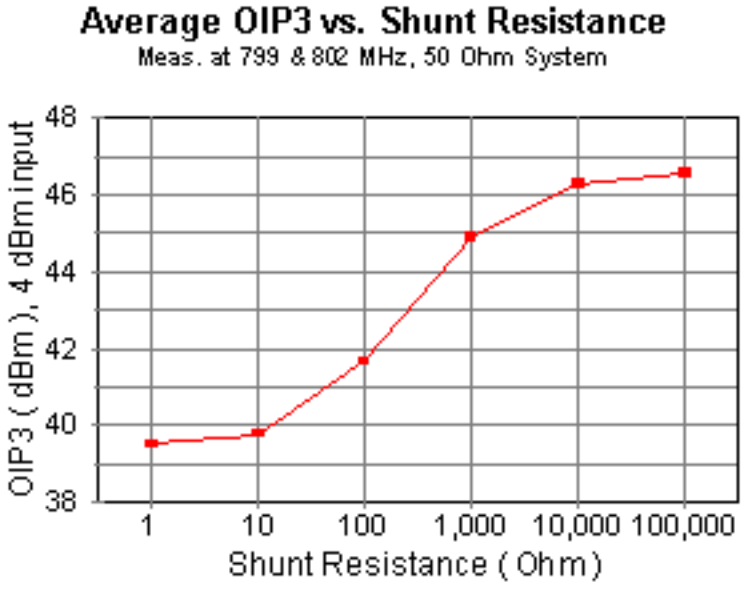

Figure 17-2

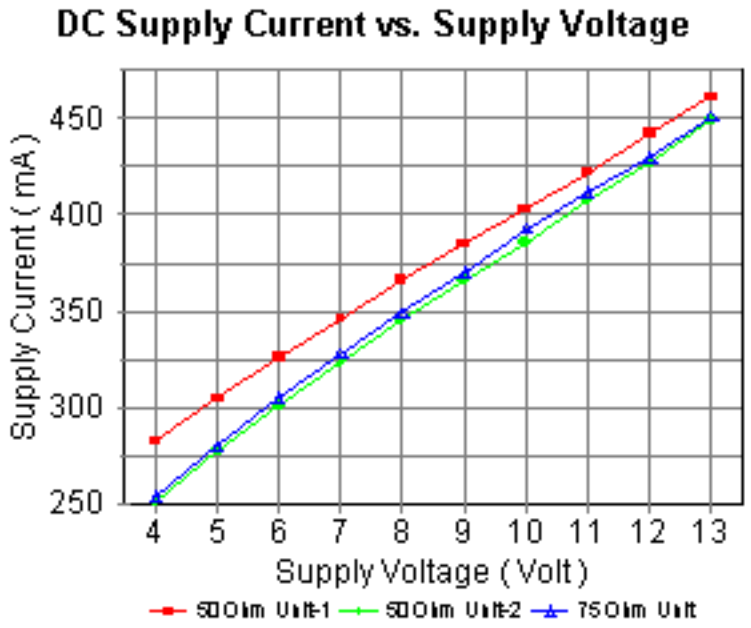

Figure 18

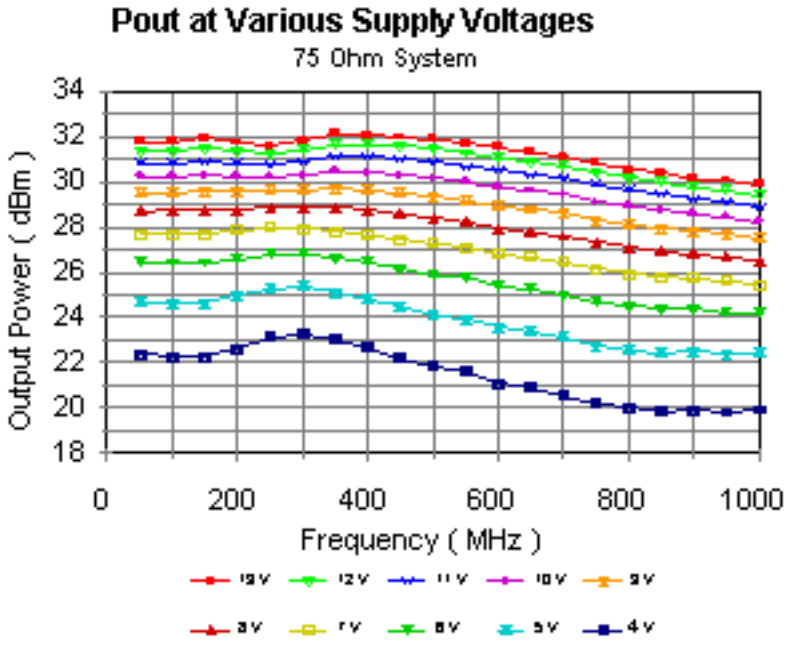

Figure 19-1

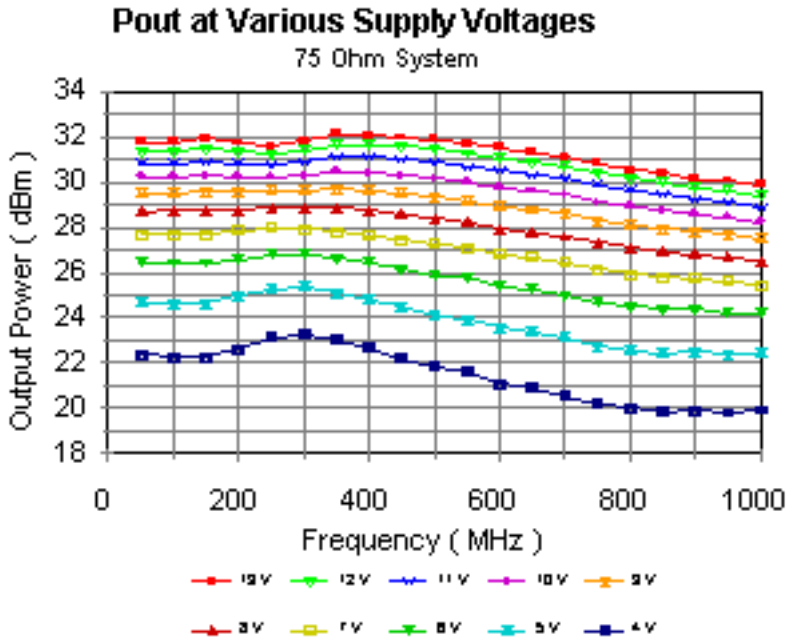

Figure 19-2

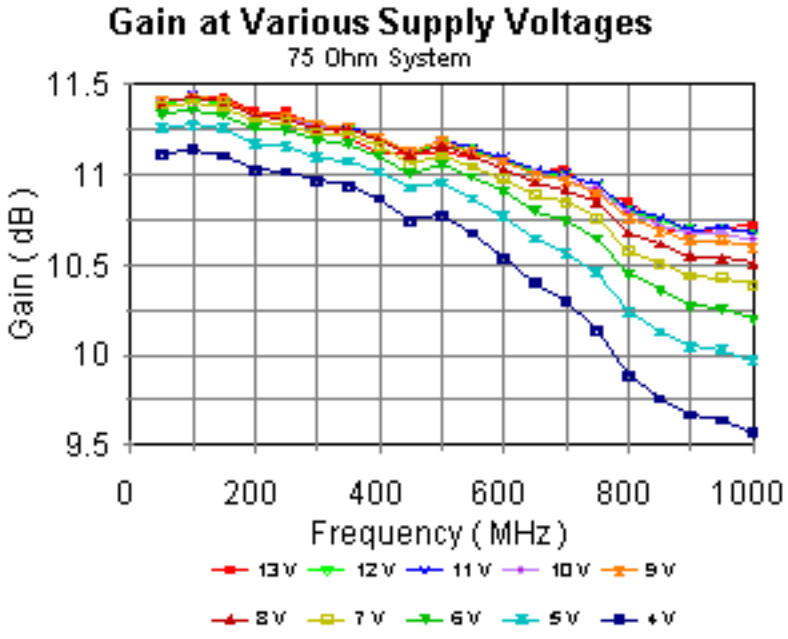

Figure 20-1

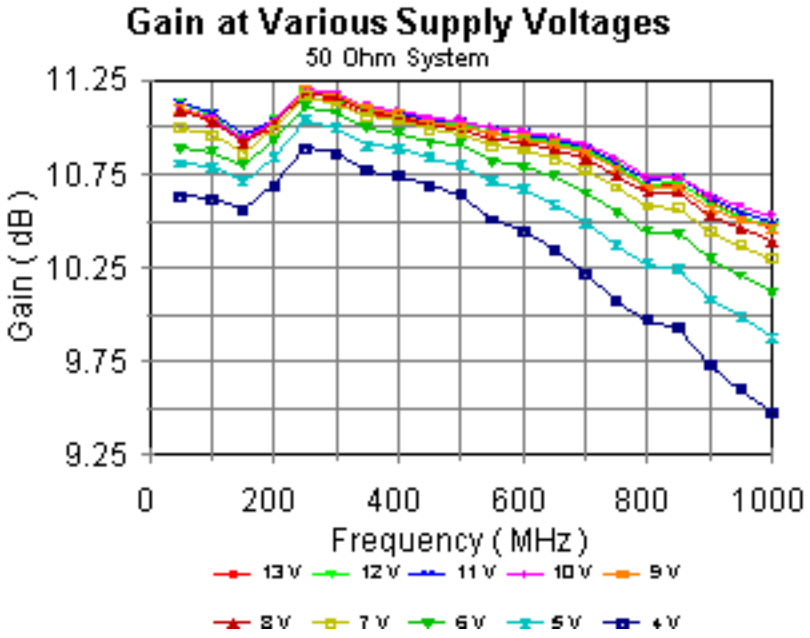

Figure 20-2

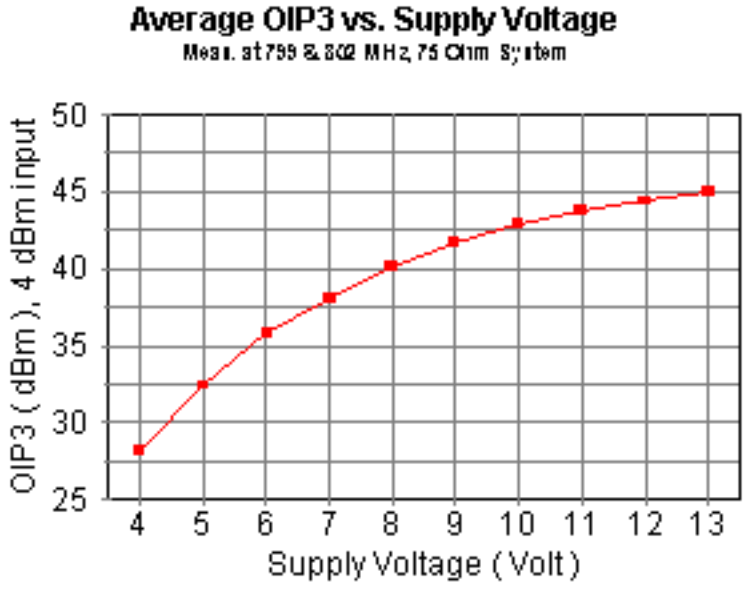

Figure 21-1

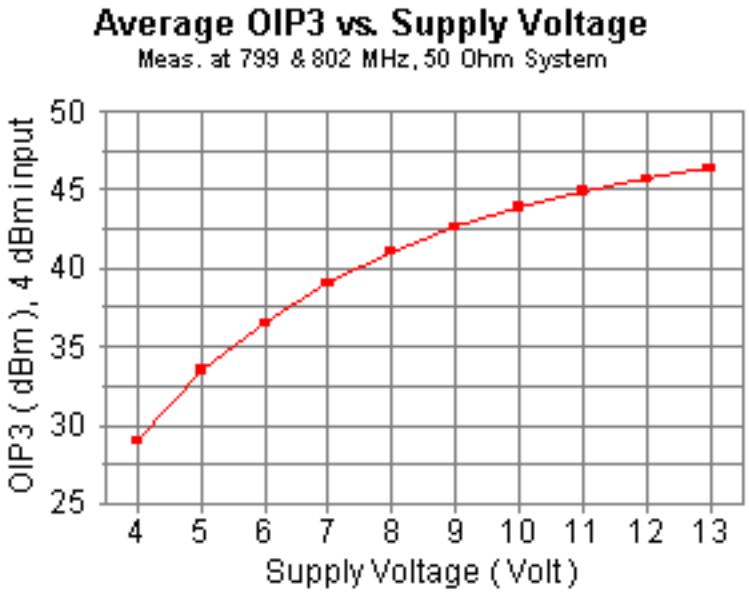

Figure 21-2

Last Updated: 09/08/1999